Fact Sheet PRP-1 Core

ZHAW offers an implementation of the Parallel Redundancy Protocol (PRP according to IEC 62439-3 / 2012) as a VHDL IP core.

Features

The ZHAW PRP-1 Core is an IP to implement a PRP Redundancy Box (RedBox) on a FPGA. It is designed to be ported easily to different platforms. Version 1 of the PRP protocol is implemented, which is not compatible with the older version of the standard (called PRP-0 or IEC 62439-3 / 2010).

Capabilities:

- Dynamic frame buffer allocation (page manager)
- 100 Mbit/s full-duplex Ethernet (i.e. no half-duplex nor 10 Mbit/s operation)
- 128 proxy nodes supported
- Wishbone interface for accessing configuration status registers
- CPU interface for receiving and sending frames can be Ethernet (MII) or Wishbone
- Configurable frame buffer size and queue length
- Duplicate detection with configurable size and aging time
- MAC address filtering (8 filter masks for interlink, 6 for CPU)
- 50 MHz system clock, 100 MHz duplicate detection clock
- Can pass extra data with frames (e.g. to implement IEEE1588 PTP clock)

The PRP-1 Core is interface-compatible with the ZHAW HSR Core, sharing a big part of the code base. PRP-1 requires fewer FPGA resources, but shares some of the HSR specific infrastructure.

Delivery

The delivery consists of:
- Source code in VHDL with VHDL test bench
- Reference implementation for an Altera Cyclone III FPGA
- Source code of the demo Software, including an Ethernet driver for Nios2-Linux
- Documentation in English

In order to run the reference implementation a suitable hardware kit is available. The board is delivered as a ready to run PRP RedBox. It is equipped with a Cyclone III FPGA, four Ethernet PHYs, RAM and Flash. The NIOS II softcore CPU (with MMU) provides basic functions such as initialization of the device and sending supervision.

The documentation includes a quickstart guide and a detailed manual. The quickstart guide describes the reference implementation, how to rebuild it and how to run the testbench. The manual describes the Core interfaces, the process of porting to a new platform, the purpose and working of internal modules, the register set and most of the internal signals.
Overview
The ZHAW PRP Core provides a byte-oriented signal interface to connect to 100 Mbit/s full-duplex Ethernet. To connect to a standard PHY, a conversion to MII is provided. To connect to the CPU for supervision, management, and link-local protocols, a Wishbone interface is provided.

The reference implementation is shown below.

Configuration Variant
The IP Core can be configured to use FPGA-Internal RAM. It is also possible to use an external CPU connected via Ethernet. However the CPU still needs access to the registers of the IP Core.
Porting

There are two basic regions in an FPGA design using the ZHAW PRP Core. The first region is the PRP Core itself. This block is designed to be used without modification, independent of the networking interfaces and the choice of a CPU. It can be configured through the use of constants at synthesis time and via registers at runtime.

The second region consists of the modules connected directly to the PRP Core. This is where all the platform dependent code is located at. It includes the Ethernet interfaces (e.g. the conversion from the byte interface to MII), a data RAM for storing the frame payload, and the CPU.

Contact

<table>
<thead>
<tr>
<th>Address</th>
<th>Institute of Embedded Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Technikumstr. 9</td>
</tr>
<tr>
<td></td>
<td>P.O. Box</td>
</tr>
<tr>
<td></td>
<td>CH-8401 Winterthur</td>
</tr>
<tr>
<td>Internet</td>
<td><a href="http://www.ines.zhaw.ch/">http://www.ines.zhaw.ch/</a></td>
</tr>
<tr>
<td>E-Mail</td>
<td><a href="mailto:info.ines@zhaw.ch">info.ines@zhaw.ch</a></td>
</tr>
<tr>
<td>Phone</td>
<td>+41 58 934 75 25</td>
</tr>
<tr>
<td>Fax</td>
<td>+41 58 935 75 25</td>
</tr>
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