Zürcher Hochschule für Angewandte Wissenschaften
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Fact Sheet HSR Core

ZHAW offers an implementation of the High-availability Seamless Redundancy Protocol (HSR according to IEC 62439-3 / 2012) as a VHDL IP core.

Features

The ZHAW HSR core is an IP to implement an HSR Redundancy Box (RedBox) on a FPGA. It is designed to be ported easily to different platforms.

Capabilities:

- Cut-through switching between HSR ports (ports A and B)
- Forwarding delay around 6 us between port A and B (assuming empty queues)
- Dynamic frame buffer allocation (page manager)
- 100 Mbit/s full-duplex Ethernet (i.e. no half-duplex nor 10 Mbit/s operation)
- One VLAN tag supported, no priority queuing
- 128 nodes supported in HSR-SAN mode
- Wishbone interface for accessing configuration status registers
- CPU interface for receiving and sending frames can be Ethernet (MII) or Wishbone
- Configurable frame buffer size and queue length
- Duplicate detection per TX port with configurable size and aging time
- MAC address filtering (8 filter masks for interlink, 6 for CPU)
- 50 MHz system clock, 100 MHz duplicate detection clock

Modes of operation:

- RedBox in HSR-SAN mode (normal mode)
- RedBox in HSR-HSR mode (to implement a QuadBox)
- RedBox in HSR-PRP mode (to realize a HSR/PRP-1 transition)

A variant of the HSR Core supports IEEE 1588 (i.e. PTP):

- One-step operation (forwarding delay between A and B is 7 us in this case)
- Hybrid clock, i.e. peer-to-peer TC in the ring path, BC between ring and interlink

Delivery

The delivery consists of:
- Source code in VHDL with VHDL test bench
- Reference implementation for an Altera Cyclone III FPGA
- Source code of the demo Software, including an Ethernet driver for Nios2-Linux
- Documentation in English

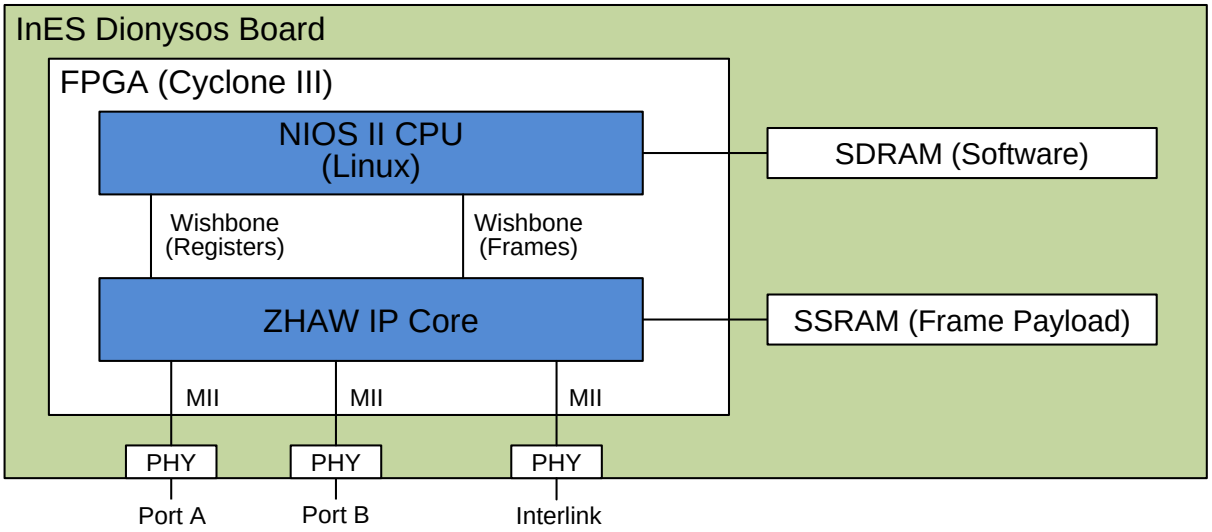
In order to run the reference implementation a suitable hardware kit is available. The board is delivered as a ready to run HSR RedBox. It is equipped with a Cyclone III FPGA, four Ethernet PHYs, RAM and Flash. The NIOS II softcore CPU (with MMU) provides basic functions such as initialization of the device and sending supervision.

The documentation includes a quickstart guide and a detailed manual. The quickstart guide describes the reference implementation, how to rebuild it and how to run the testbench. The manual describes the Core interfaces, the process of porting to a new platform, the purpose and working of internal modules, the register set and most of the internal signals.

Overview

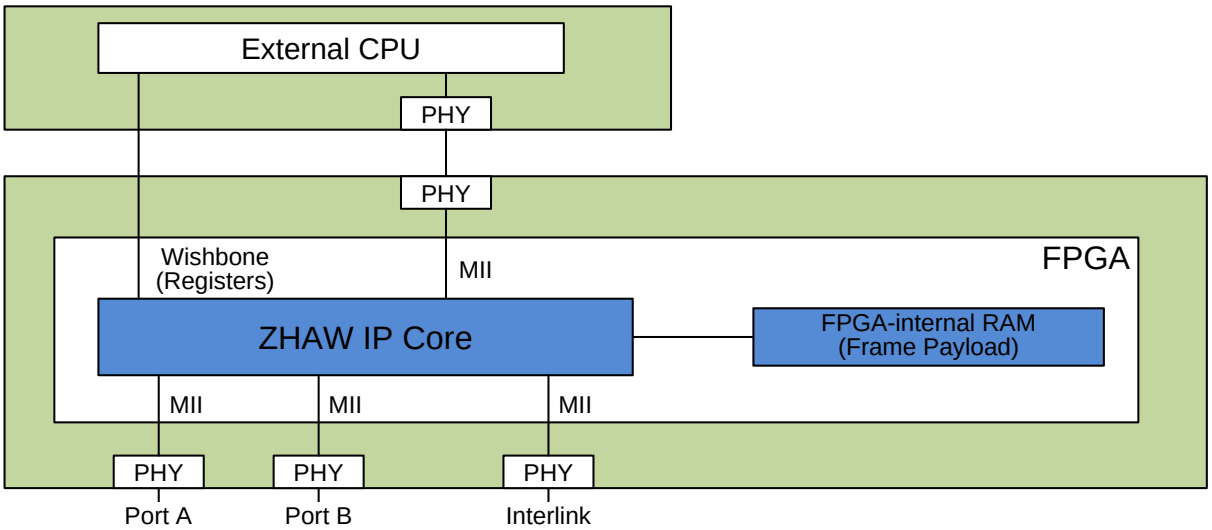
The ZHAW HSR Core provides a byte-oriented signal interface to connect to 100 Mbit/s full-duplex Ethernet. To connect to a standard PHY, a conversion to MII is provided. To connect to the CPU for supervision, management, and link-local protocols, a Wishbone interface is provided.

The IP Core implements the switching rules according to IEC 62439-3 section 5 and supports cut-through switching for low latency on the ring ports. The reference implementation is shown below.



Configuration Variant

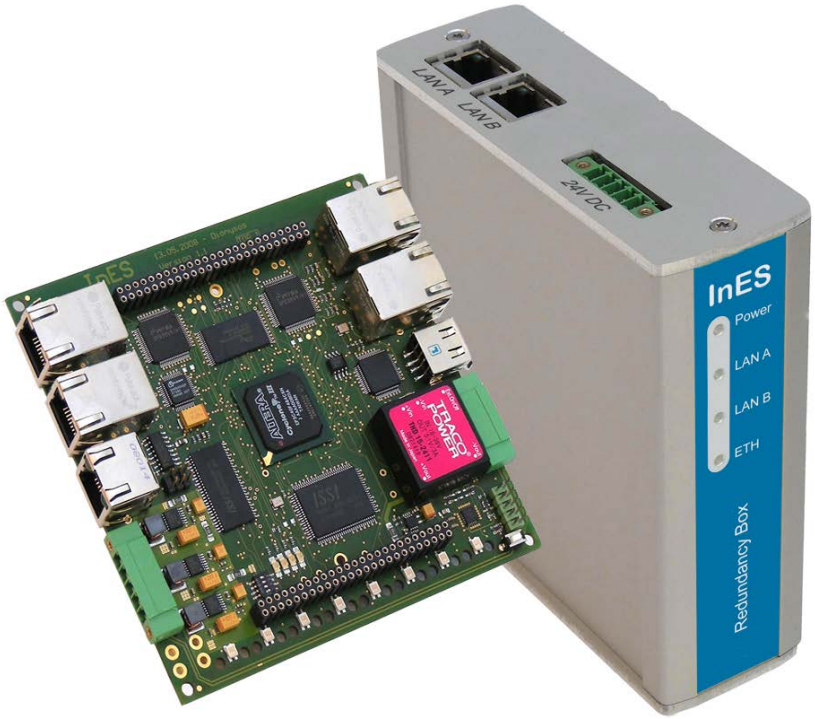
The IP Core can be configured to use FPGA-Internal RAM. It is also possible to use an external CPU connected via Ethernet. However the CPU still needs access to the registers of the IP Core.



Porting

There are two basic regions in an FPGA design using the ZHAW HSR Core. The first region is the HSR Core itself. This block is designed to be used without modification, independent of the networking interfaces and the choice of a CPU. It can be configured through the use of constants at synthesis time and via registers at runtime.

The second region consists of the modules connected directly to the HSR Core. This is where all the platform dependent code is located at. It includes the Ethernet interfaces (e.g. the conversion from the byte interface to MII), a data RAM for storing the frame payload, and the CPU.



Ready to run reference implementation on ZHAW evaluation kit.

Contact

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