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Configuration / Registers	PROFINET Stack	MRP	Frag.	Application
	Mailboxes – Frame Buffers Mgmt. RTC1 RTC2 IP			Frame - Mbx. / Buffers
	Sync. / Delay Measurement		RTC3	
	Offset & Drift Control / Clock	Synchronizat Non Real Time Real Time Forwar	ding prwarding	
	Time Stamping / on-the-fly Time - Stamp Insertion	Dynami	cking MAC	
		РНҮ		РНҮ

What is easyIRT?

easyIRT is a PROFINET IRT communication controller written completely in VHDL ready for synthesis in an FPGA. Supporting advanced features like Dynamic Frame Packing, easyIRT supports cycle times down-to 31.25us. easyIRT can be easily combined with other IP's to build entire System on Chip (SoC) solutions.

easyIO Features

- Optimised for Xilinx Zynq
- Compatible to all PROFINET stacks, (f.i. Molex)
- IRT cycle times as low as 31.25us.
- Adaptable for other Real Time Ethernet Protocols
- Available in binary and source code versions, royalty free

Where to get easyIRT?

easyIRT is available for licensing, including support and maintenance, from Enclustra GmbH, FPGA Solution Center, Technoparkstrasse 1, CH-8005 Zurich, Switzerland. Tel: +41 43 343 39 43, <u>info14@enclustra.com</u>

Institute of Embedded Systems P.O. Box 805 | CH-8401 Winterthur +41 58 934 75 25 | info.ines@zhaw.ch



Full speed Enterprise traffic over Profinet in FPGA

In most Profinet solutions the handling of real-time (RT) and non-realtime (NRT) traffic is encapsulated in one device (ASIC, FPGA, etc.). This often causes compromises in bandwidth and makes users run a separate network for enterprise traffic.

The novel Hardware Offloading architecture separates RT and NRT traffic in hardware and allows full control of the NRT traffic in terms of speed and operating system.



Field of Application

The Hardware Offloading architecture is especially suited for FPGA designs with soft and hard CPUs. Enclustra offers a solution for Xilinx Zynq-7000 with the following features:

- Profinet RT encapsulated on a Microblaze CPU
- User can use both ARM A9 cores for NRT traffic and its own purposes
- NRT traffic driver for Linux and eCos available

easyIRT Profinet communication core

The Profinet communication core is fully written in VHDL and ready for synthesis in an FPGA. It can be licensed as one processor solution or as Hardware offloading solution. Both architectures offer the following features:

- Low cycle times (down to 31.25us)
- Dynamic frame packing
- Binary/source code available, royalty free

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Wind Turbine Control-Architecture Re-Design

Wind generated energy has become a widely accepted form of green energy generation. Currently energy generation is directly fed into the distribution network which results in large reactive power losses. Additionally turbines have historically single controllers controlling a particular aspect of the turbine. To make utilisation of generated power more efficient the power injection into the distribution net was to be synchronised with the phase of the distribution network. To reduce costs consolidation of turbine control in one controller system was required.



Architecture Re-Factoring

For the consolidation of control architectures within the wind turbine PROFINET was chosen. The system architecture was finalised with two network segments at cycle times of 10 ms and 125 us running on a Simotion P350 motion controller from Siemens. Since Dynamic Frame Packing was required and the PROFINET stack didn't support IRT below 250 us, the stack had to be modified.

easyIRT Profinet communication core

With the inverters being controlled at cycle times of 125us it is now possible to de-couple energy generation from energy injection into the power transmission lines.

To minimise reactive loss the inverters are controlled two stage. Once for generating the power from the turning turbine – power which is stored temporarily – and a second where the injection of that stored power into the distribution network is synchronised with the phase of that network.

Institute of Embedded Systems P.O. Box 805 | CH-8401 Winterthur +41 58 934 75 25 | info.ines@zhaw.ch School of Engineering

Dynamic Frame Packing in Industrial Applications using COTS Components

For a high speed 6-axis motion control system using cycle times of 62.5us PROFINET Dynamic Frame Packing (DFP) was required. Equally the use of a standard controller was specified. Since standard PROFINET controllers don't support cycle times this low a standard controller needed to be adapted.



Architecture Considerations

A series of axis controllers was used. The first in the line was a synchronization master to the rest of the axis-controllers. It transmitted DFP frames to these controllers and sent the received frames as one frame to the standard Siemens Microbox controller. This controller needs to run the positioning algorithm. To do this the driver needed to be modified.

Driver modification

The driver could be modified and optimised so that only 5 us were spent processing code and 24 us required for interrupt latencies and the like. This left 33 us for processing the position control algorithm across the 6 axis.

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Innovation in Communications

InES

InES has become, internationally, the premier research and design institute in the field of industrial communication. Known for its rigorous coverage of all aspects of communication theory, technology and industrial application, InES is the ideal partner for developing and implementing solutions for high-performance communication problems.

Pure Research

Various research projects covered by our 5 focus groups include on-going research into embodied, situated and pheromone communication techniques for bio-inspired robotics. Energy harvesting techniques for autarkic systems, design techniques for embedded systems and coprocessor design are further examples of a comprehensive body of research activities in the field of embedded systems.

Applied Research

Feasibility studies allow the investigation of particular aspects of communication technology for furtherance to specification bodies or for further applied research. Examples include the conceptualisation and standardisation of IEEE1588 and the redundancy protocol HSR. A second example is the research of architectures for ensuring highly available but functionally safe and dependable systems.

Industrial Implementations

InES has industrial-quality completed many communication implementations. Examples are IEEE 1588 V2.0 stacks in both hardware and software. Implementations of MRP, PRP and HSR redundancy protocols. easyIRT; single-chip very fast PROFINET а IRT implementation. POWERLINK stacks and conformance test software, DSL redundancy communication systems for highly-reliable rail signalling systems. Multi-Media transport over IP.

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