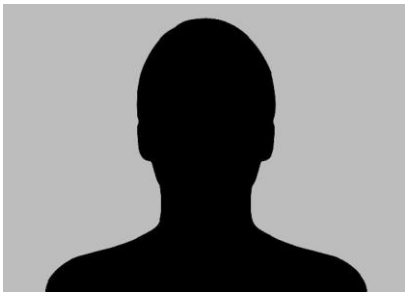
Zurich University
of Applied Sciences

School of
Engineering

InES Institute of
Embedded Systems

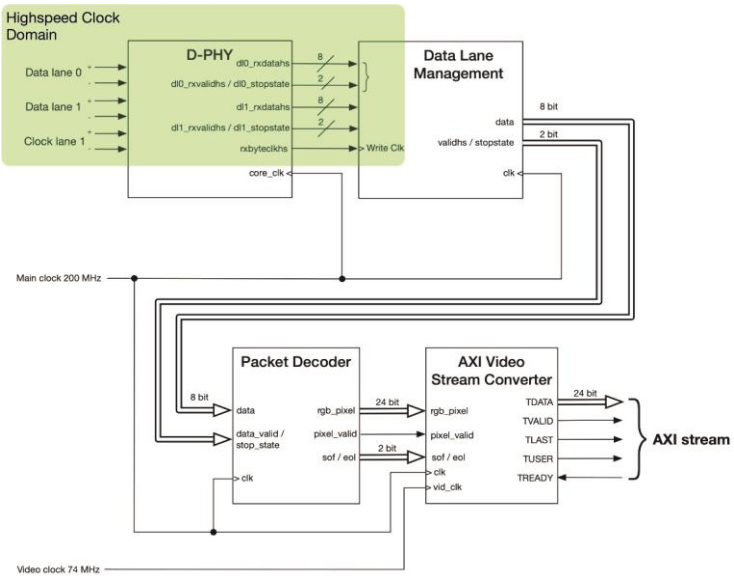
Entwicklung eines FPGA Blocks zur umwandlung eines Camera Interfaces (CSI) zum AXI-4 stream Protokol



Diplomand
Andreas Helmut Winter

Dozent
Hans-Joachim Gelke

In this thesis a hardware implementation of the MIPI (Mobile Industry Processor Interface) Camera Serial Interface (CSI) was developed. The CSI connects the camera with the System On Chip (SoC) in mobile devices. Since the complete specification of this interface is complex, only a certain subset was implemented. Starting with an overview of the protocol stack, certain features and functionalities of the interface were discussed in detail. The protocol stack itself provided the framework along which the implementation was performed. Various functionalities already provided in the FPGA fabric helped to solve certain problems. For example, the transition between clock domains could be solved relatively easily by using these functionalities. The development itself was done in VHDL and the hardware platform was a powerful Xilinx Zync UltraScale.



Block diagram CSI to AXI Stream