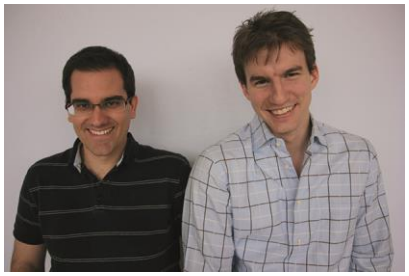
Zurich University
of Applied Sciences

School of
Engineering

InES Institute of
Embedded Systems

Algorithmen zur Bildoptimierung von medizinischen Kameras



Diplomierende
David Blatter
Andreas Stucki

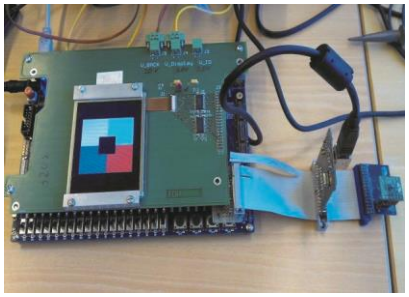
Dozent
Hans-Joachim Gelke

To display a videostream from a mini camera on a TFT display there are several hurdles to take. In the course of this bachelor thesis they were taken successfully.

Based on its short dimensions, a mini camera was choosen as the image taking element of a medical endoscope. With its 400x400 CMOS sensor array, the camera is mapping parts of its environement as a bayer pattern array. The output-stream has a frame rate of 30 fps (frames per second).

To display this stream, the industrial partner selected a 320x240 and a 640x480 TFT display from the manufacturer ORTUSTECH with a frame rate of 60 fps and RGB pixeldata as input.

Considering these specifications a FPGA was choosen to bypass the differences between the two ends of this medical ensodcope. On one hand there was a different frame rate and on the other hand there were differing data formats. With a 3 block design within the FPGA these differences were eliminated.



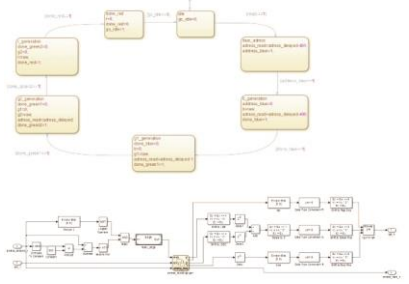
This picture shows from left to right the display mounted on the evaluation board, the OV hardware (digitalization of the camera signal) and the camera itself. A test picture generated inside the Input-Handler is visible on the display.

Input-Handler
This conversion block, which was implented using Mathworks, is reading the frame data from the spy camera and buffers it line by line. Next the red, green and blue pixels were transformed into RGB pixels and forwarded to the SRAM-Controller. The Input-Handler also generates the corresponding addresses to the RGB pixels based on the input timing generated inside the spy camera.

SRAM-Controller
Receives RGB pixels with the corresponding address from the Input-Handler and stores it, so that the Output-Handler can read it out for the output stream to the display. This block bridges the two different frame rates, allowing a total of two complete pictures to be saved in the SRAM. While the Input-Handler stores one full frame, the Output-Handler can read out the already completed picture in the SRAM twice. This line of action provoces a delay of one input frame.

Output-Handler
Generates the timing for the currently used display and places, pending on the actual position inside a frame, read requests to the SRAM-Controller for streaming out the pixel data.

These blocks were realized and validated during this bachelor thesis.



A part of the conversion logic from RAW to RGB format is illustrated at the bottom of the picture. The flow of the state machine (placed in the middle of the logic) is visualized in the upper diagram.