## School of **ZN**

Engineering InES Institute of

**Embedded Systems** 

## Android on PSOC

Until now, it has not been very common to have Android running as an operating system on an FPGA. Therefore, it is the aim of this bachelor thesis to investigate whether or not Android works properly on an embedded processor in an FPGA. This paper is based on the preceding project thesis «Android on PSOC», following up the same objectives.

The hardware composition of the project had to be upgraded with several interfaces, such as SD Card Controller, Ethernet and the touch input. The expansions had to be made in the Linux Kernel as well. Not only the integration of the interfaces but also a few modifications for Android compatibility were necessary in the Kernel. On top of that the Android source had to be configured and compiled for the Nios II softcore processor.

While the hardware configuration in Altera's system integration tool Qsys was easily managed, the Kernel as well as the Android compilation were very challenging. Since there are many engineers working with Linux on an Altera FPGA, it was possible to obtain professional assistance for setting up the Kernel. However, the information had to be gathered together from all different kinds of sources; Mr. Patrick Heeb, a senior engineer at Noser Engineering, as well as different forums in the internet have been very helpful during this process. Contrary to expectations, Android is not independent from the processor type. Therefore, many adjustments had to be made in the Android source code.

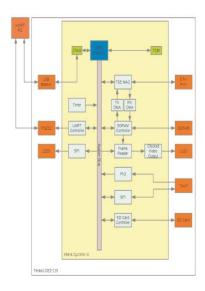
Even though the Linux Kernel and selected programs such as MicroWindows run on the target device, Android could not be fully ported on the evaluation board in the available time.

In conclusion it must be said that it might be possible to have Android running on a Nios II softcore CPU but for reasons mentioned in this paper the authors doubt that it would be fast enough to work fluently, keep up with or even compete against a CPU like a x86 or an ARM core.



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In our Bachelor thesis we used a tPad Multimedia Development Kit from Terasic which is based upon a DE2-115 Development Board. It features a Cyclone IV FPGA from Altera, 128MB SDRAM, 2MB SRAM, 8MB parallel und 8MB serial Flash (EPCS64). It's equiped with a lot of peripherials such as VGA, USB, PS/2, Ethernet PHY and many more.