Electrothermal simulation of large-area semiconductor devices

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LAOSS CTI project (2016–2018)

The results presented here were obtained within the

Large Area Organic Semiconductor Software (LAOSS)

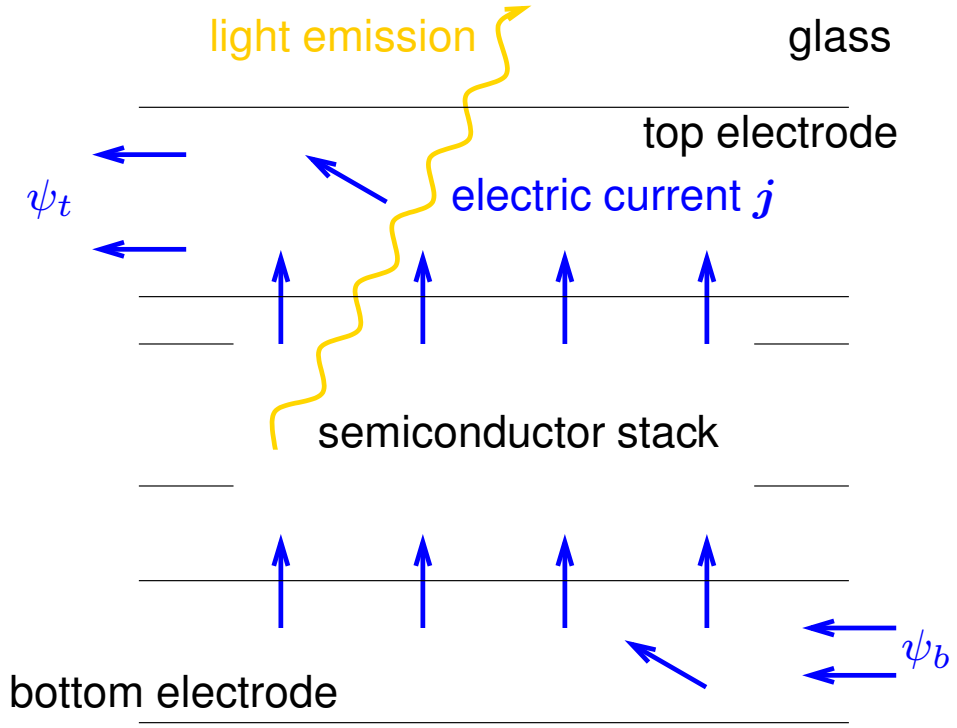
project, funded by the Swiss Commission for Technology and Innovation (CTI; now Innosuisse) from 2016–2018.

Within this research project a prototype model was developed at the ICP for testing new ideas, some of which went into Fluxim's Laoss software.

A "large-area device" is a device in which the lateral charge transport in the electrodes has a significant effect on the device performance.

Charge transport and heat transfer

Multilayer semiconductor stack between two electrodes (e. g. OLED):



- charge transport governed by

  Ohm's law: $\boldsymbol{j} = -\sigma \nabla \psi \ [\mathrm{Am}^{-2}]$

  electrical conductivity $\sigma \ [\mathrm{Sm}^{-1}]$

  electric potential $\psi \ [\mathrm{V}]$

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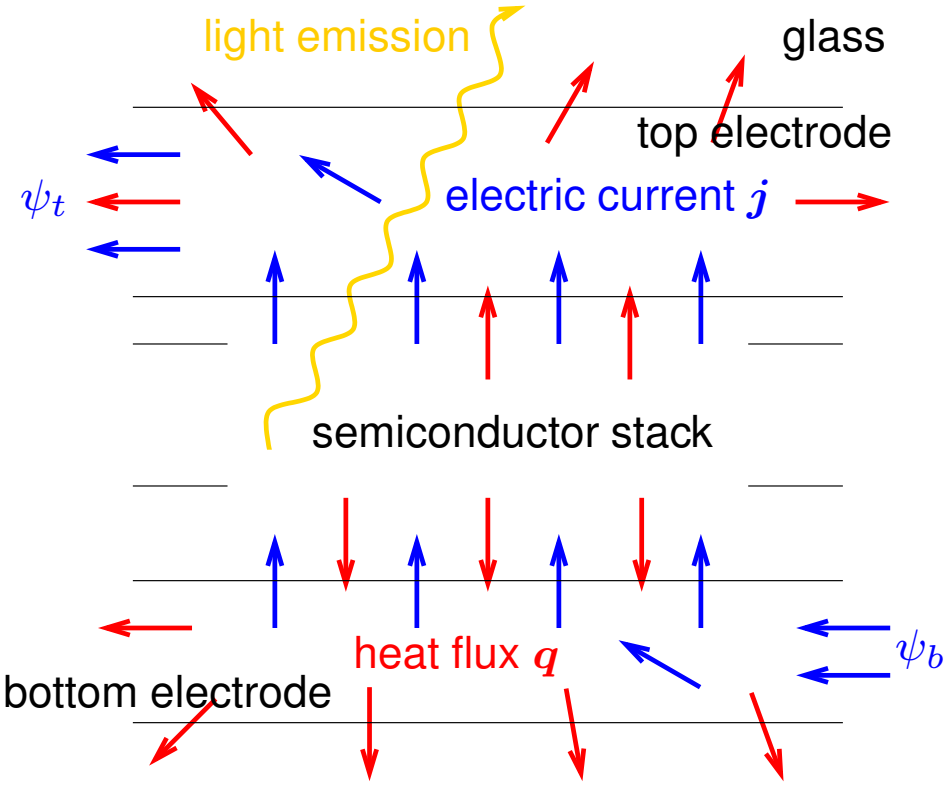

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- heat transfer governed by

  Fourier's law: $\boldsymbol{q} = -\lambda \nabla T \ [\mathrm{Wm}^{-2}]$

  thermal conductivity $\lambda \ [\mathrm{W(mK)}^{-1}]$

  temperature $T \ [\mathrm{K}]$

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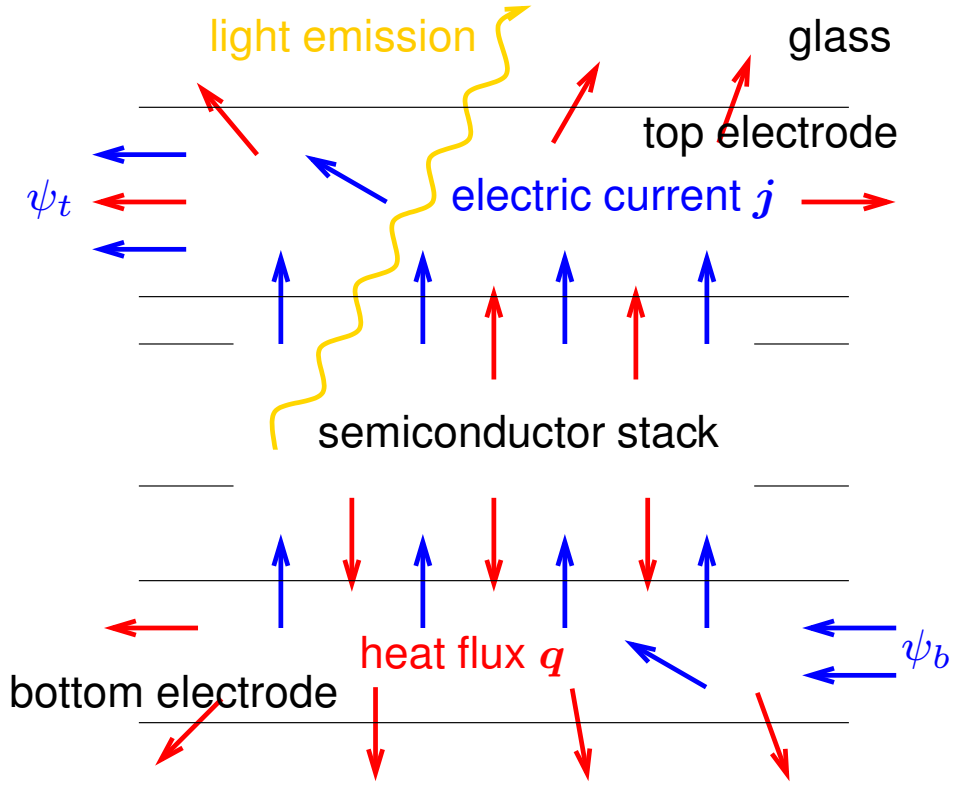

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- electrical $\rightarrow$ thermal coupling via Joule heating $\propto \sigma |\nabla \psi|^2 \ [\mathrm{Wm}^{-3}]$.
- thermal $\rightarrow$ electrical coupling via temperature-dependent charge transport properties, especially in the semiconductor stack.

Dimensional reduction

Instead of using a full three-dimensional (3D) model for the charge transport and heat transfer in the semiconductor device we combine

- a two-dimensional (2D) model for each thin-film electrode with
- a zero-dimensional (0D) model for the semiconductor stack.

The coupled 0D-2D approach is important for reducing the computational cost since

- typical layers are very thin compared to their lateral dimensions (lateral $\sim 10^{-3}\,\mathrm{m} \sim 10^{-2}\,\mathrm{m}$, vertical $\sim 10^{-8}\,\mathrm{m} \sim 10^{-6}\,\mathrm{m}$) and
- the smallest length scale in the computational domain usually determines the maximum mesh size in a discretization (stability).

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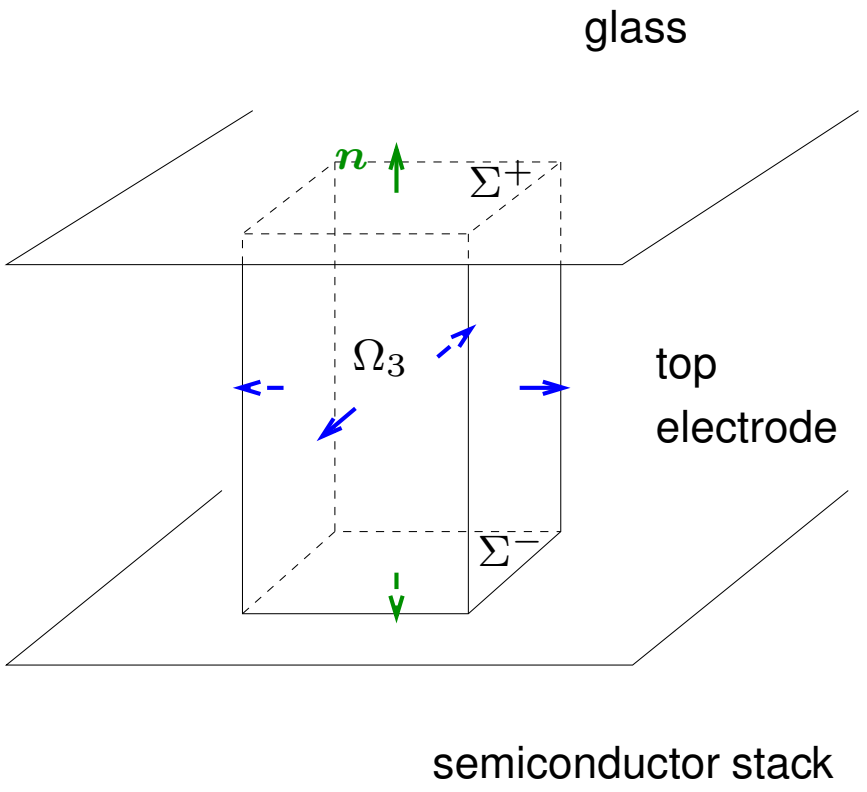
3D: N vertical degrees of freedom (dofs) $\rightsquigarrow \sim (10^5 N)^2$ lateral dofs $\rightsquigarrow \sim 10^{10} N^3$ dofs in total!

Dimensional reduction in top electrode (1)

Special control volume with faces Σ^+ and Σ^- at the top and bottom faces of the (top) electrode, where the outward electric current density is known. Steady-state equations:

$$\begin{aligned} \operatorname{div} \boldsymbol{j}_3 &= 0 \quad \text{in } \Omega_3, \\ \boldsymbol{j}_3 \cdot \boldsymbol{n} &= 0 \quad \text{on } \Sigma^+, \\ \boldsymbol{j}_3 \cdot \boldsymbol{n} &= -j_s \quad \text{on } \Sigma^-. \end{aligned}$$

$$\boldsymbol{j}_3(x,y,z) = \begin{pmatrix} j_{3,x}(x,y,z) \\ j_{3,y}(x,y,z) \\ j_{3,z}(x,y,z) \end{pmatrix}$$

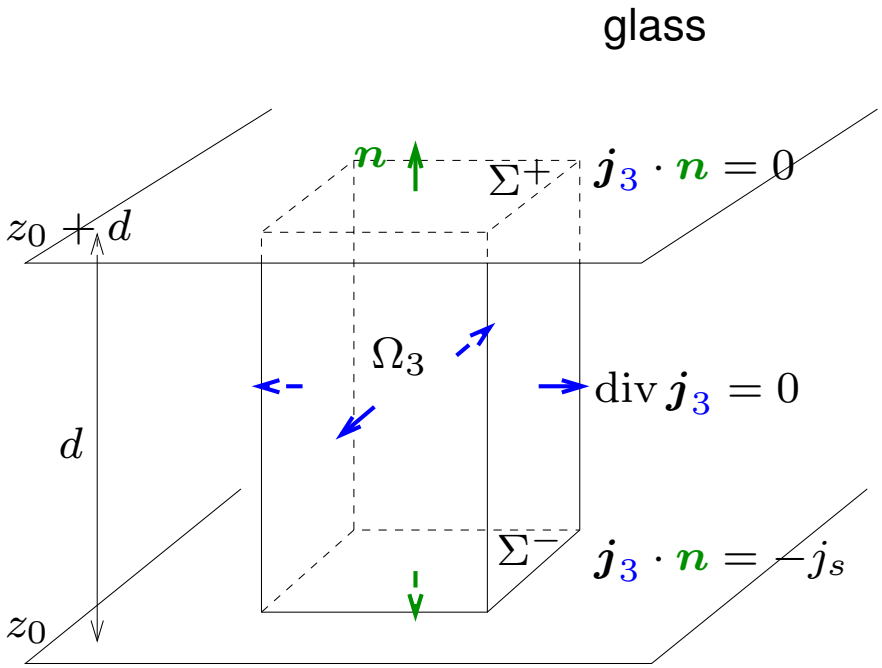


j_s: current density $[\mathrm{Am}^{-2}]$ out of the semiconductor stack into the top electrode, orthogonal to the interface.

Dimensional reduction in top electrode (2)

$\operatorname{div} \boldsymbol{j}_3 = 0$, integrate in z-direction:

$$
\begin{aligned}
0 &= \int_{z_0}^{z_0+d} \operatorname{div} \boldsymbol{j}_3 \, \mathrm{d}z \\
&= \int_{z_0}^{z_0+d} \frac{\partial j_{3,x}}{\partial x} + \frac{\partial j_{3,y}}{\partial y} + \frac{\partial j_{3,z}}{\partial z} \, \mathrm{d}z \\
&= \frac{\partial}{\partial x} \int_{z_0}^{z_0+d} j_{3,x} \, \mathrm{d}z + \frac{\partial}{\partial y} \int_{z_0}^{z_0+d} j_{3,y} \, \mathrm{d}z \\
&\quad + \underbrace{j_{3,z}|_{z=z_0+d}}_{=\boldsymbol{j}_3 \cdot \boldsymbol{n}|_{\Sigma+}} - \underbrace{j_{3,z}|_{z=z_0}}_{=(-\boldsymbol{j}_3 \cdot \boldsymbol{n})|_{\Sigma-}} \\
&= \operatorname{div} \boldsymbol{j}_2 + 0 - j_s \;\Rightarrow\; \operatorname{div} \boldsymbol{j}_2 = j_s
\end{aligned}
$$



lateral current density $[\mathrm{Am}^{-1}]$

$$
\boldsymbol{j}_2(x,y) := \int_{z_0}^{z_0+d} \begin{pmatrix} j_{3,x}(x,y,z) \\ j_{3,y}(x,y,z) \end{pmatrix} \mathrm{d}z.
$$

Dimensional reduction in top electrode (3)

Ohm's law $\boldsymbol{j}_3 = \sigma \boldsymbol{E} = -\sigma \nabla \psi_3$ with the electrical conductivity σ $[\mathrm{Sm}^{-1}]$ and with the electric potential ψ_3 $[\mathrm{V}]$ (electric field $\boldsymbol{E} = -\nabla \psi_3$ $[\mathrm{Vm}^{-1}]$).

Integration in the z-direction yields lateral current density $\boldsymbol{j}_2(x, y) =$

$$\int_{z_0}^{z_0+d} \begin{pmatrix} j_{3,x}(x,y,z) \\ j_{3,y}(x,y,z) \end{pmatrix} \mathrm{d}z = -\int_{z_0}^{z_0+d} \sigma(x,y,z) \begin{pmatrix} \frac{\partial \psi_3}{\partial x}(x,y,z) \\ \frac{\partial \psi_3}{\partial y}(x,y,z) \end{pmatrix} \mathrm{d}z.$$

Assume $\frac{\partial \sigma}{\partial z} \equiv 0$, for $z_0 < z < z_0 + d$.

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$$\int_{z_0}^{z_0+d} \begin{pmatrix} j_{3,x}(x,y,z) \\ j_{3,y}(x,y,z) \end{pmatrix} \mathrm{d}z = -\sigma(x,y) d \frac{1}{d} \int_{z_0}^{z_0+d} \begin{pmatrix} \frac{\partial \psi_3}{\partial x}(x,y,z) \\ \frac{\partial \psi_3}{\partial y}(x,y,z) \end{pmatrix} \mathrm{d}z.$$

Assume $\frac{\partial \sigma}{\partial z} \equiv 0$, for $z_0 < z < z_0 + d$. Define the averaged potential

$$\psi_2(x,y) := \frac{1}{d} \int_{z_0}^{z_0+d} \psi_3(x,y,z)\, \mathrm{d}z \quad [\mathrm{V}]. \quad \text{Then } \boldsymbol{j}_2 = -{R_\square^{\mathrm{el}}}^{-1} \nabla \psi_2 \quad [\mathrm{Am}^{-1}],$$

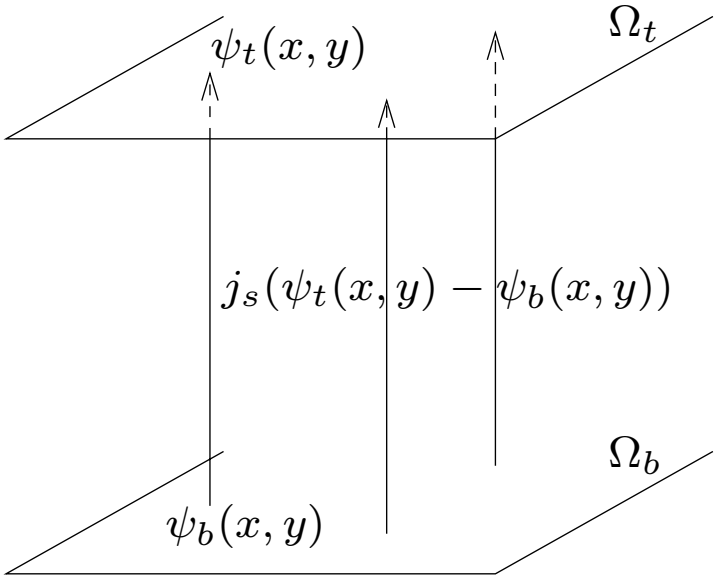
with the electrical sheet resistance $R_\square^{\mathrm{el}}(x,y) := (\sigma(x,y)d)^{-1}$ $[\Omega/\square]$. The sheet resistance is negligible in thick layers ($R_\square^{\mathrm{el}} \to 0$ as $d \to \infty$).

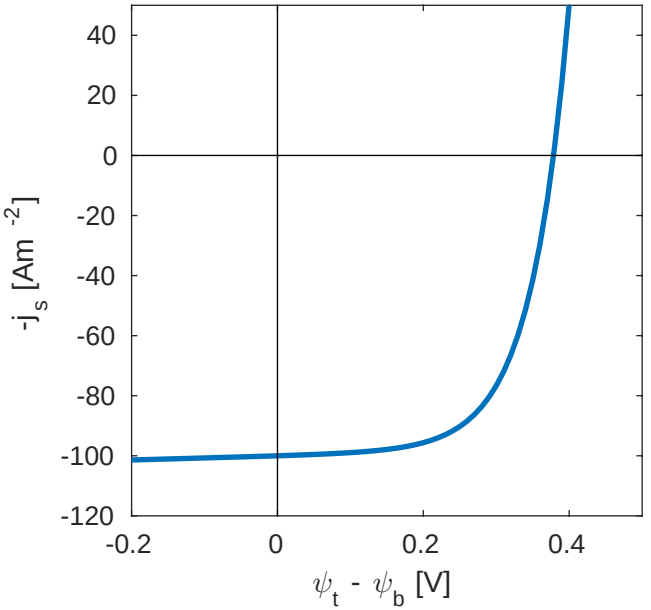
Coupled 0D-2D electrical model

2D: Combine charge balance and constitutive equations in the top electrode. Use the same procedure in the bottom electrode to obtain the system of PDEs

$$
\begin{aligned}
-\operatorname{div}({R^{\mathrm{el}}_{\square,t}}^{-1}\nabla\psi_t) &= j_s \quad \text{in } \Omega_t,\\
-\operatorname{div}({R^{\mathrm{el}}_{\square,b}}^{-1}\nabla\psi_b) &= -j_s \quad \text{in } \Omega_b.
\end{aligned}
$$

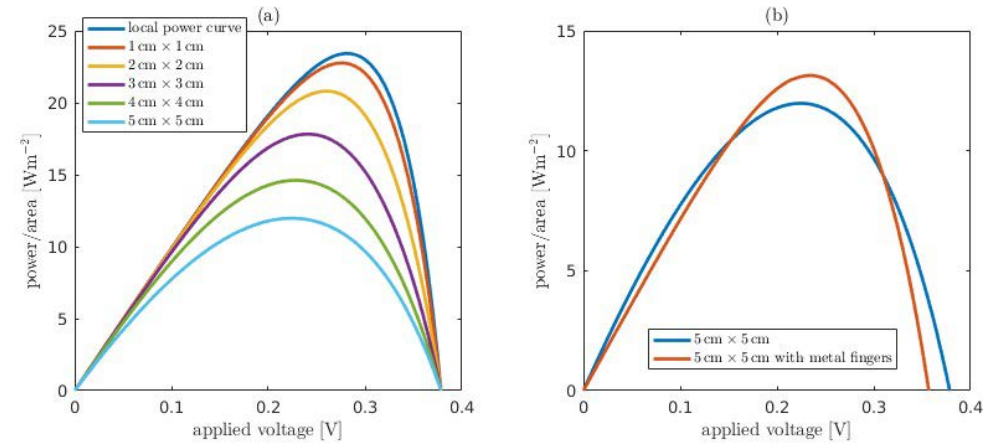
0D: In the semiconductor stack we assume no lateral current, such that the (vertical) current in the stack is determined by the potential difference between the electrodes: $j_s = j_s(\psi_t - \psi_b)$.



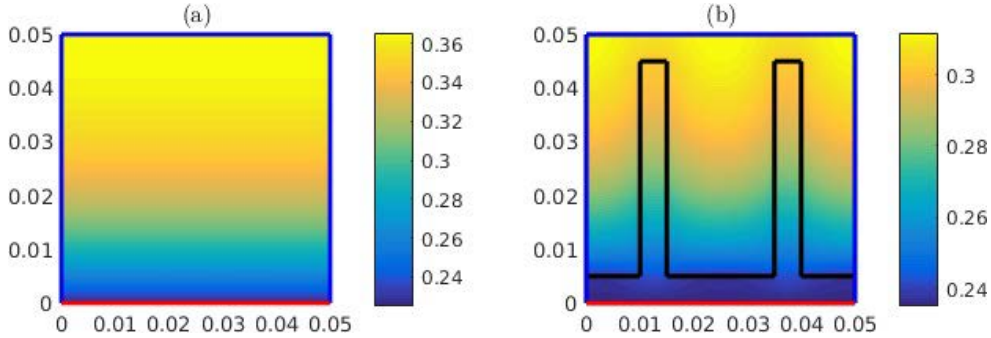


Large-area electrical solar-cell model: results

Discretization of PDEs using the finite element method (FEM), together with standard techniques such as adaptive mesh refinement.



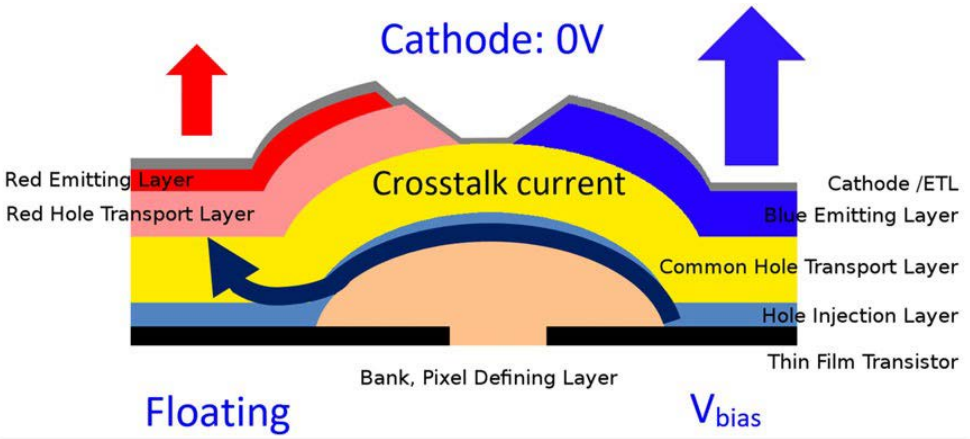
electric potential $[\mathrm{V}]$ at MPP:

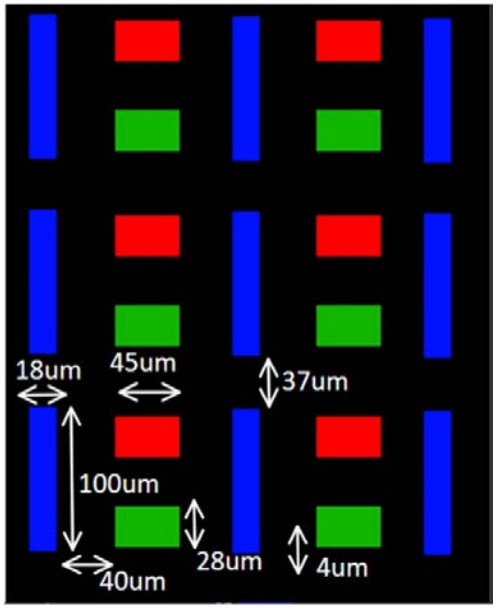


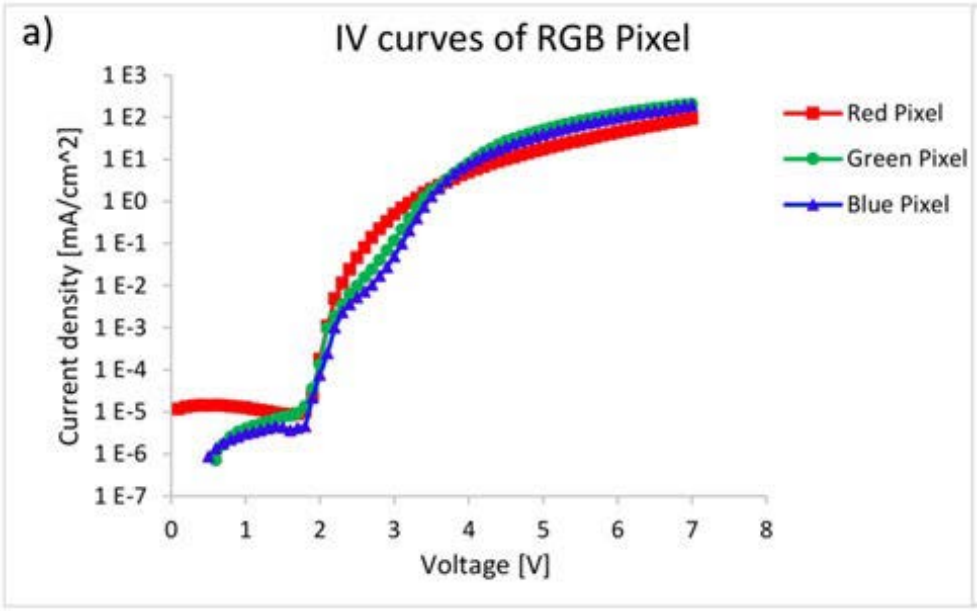
Due to the electrical sheet resistance the maximum power increases sublinearly with the device area.

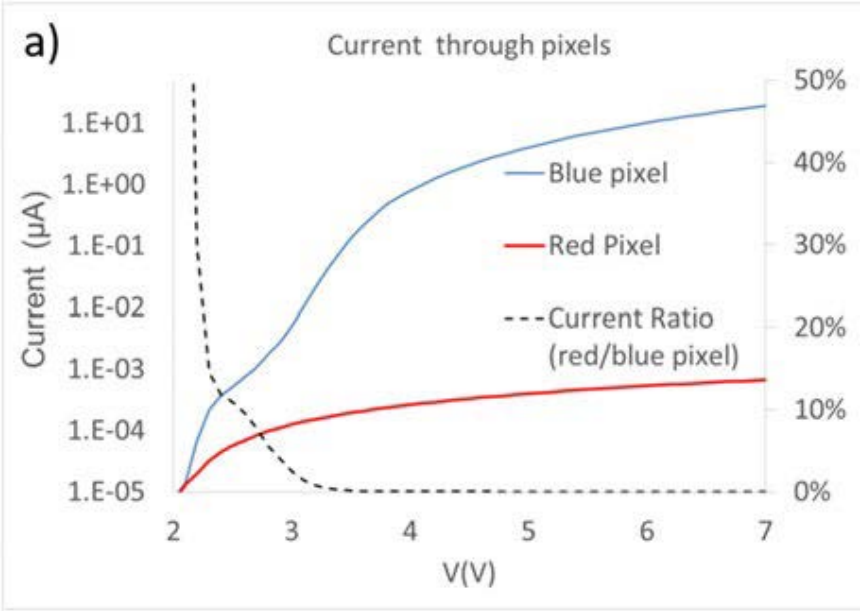
CK et al., Int. J. Multiphys. 11 (2), 2017

Large-area electrical OLED model: crosstalk









Diethelm et al., J. Inf. Disp. 19 (2), 2018; Penninck et al., J. Soc. Inf. Disp., 2018

0D-2D electrothermal model

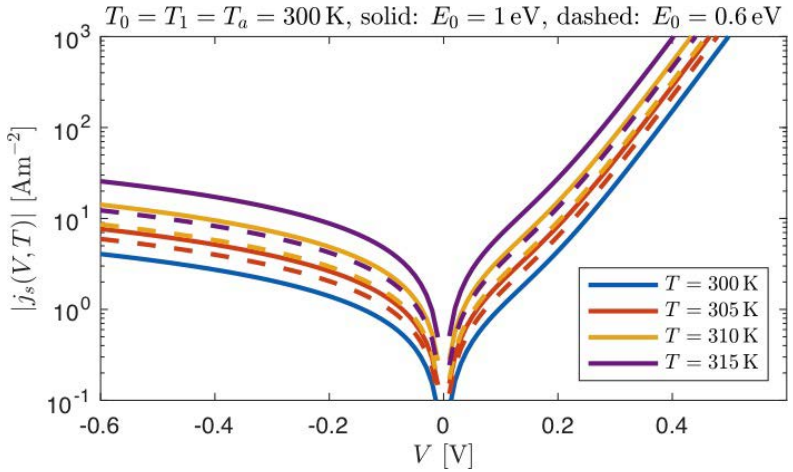
Dimensional reduction of the thermal energy balance in the top and bottom electrodes in a similar way as before, together with Fourier's law, leads to

$$
\begin{aligned}
-\operatorname{div}\left({R^{\mathrm{el}}_{\square,t}}^{-1}\nabla\psi_t\right) &= f_t^{\mathrm{el}}(\psi_t, T_t, \psi_b, T_b),\\
-\operatorname{div}\left({R^{\mathrm{th}}_{\square,t}}^{-1}\nabla T_t\right) &= f_t^{\mathrm{th}}(\psi_t, T_t, \psi_b, T_b),\\
-\operatorname{div}\left({R^{\mathrm{el}}_{\square,b}}^{-1}\nabla\psi_b\right) &= f_b^{\mathrm{el}}(\psi_t, T_t, \psi_b, T_b),\\
-\operatorname{div}\left({R^{\mathrm{th}}_{\square,b}}^{-1}\nabla T_b\right) &= f_b^{\mathrm{th}}(\psi_t, T_t, \psi_b, T_b),
\end{aligned}
$$

with the thermal sheet resistances

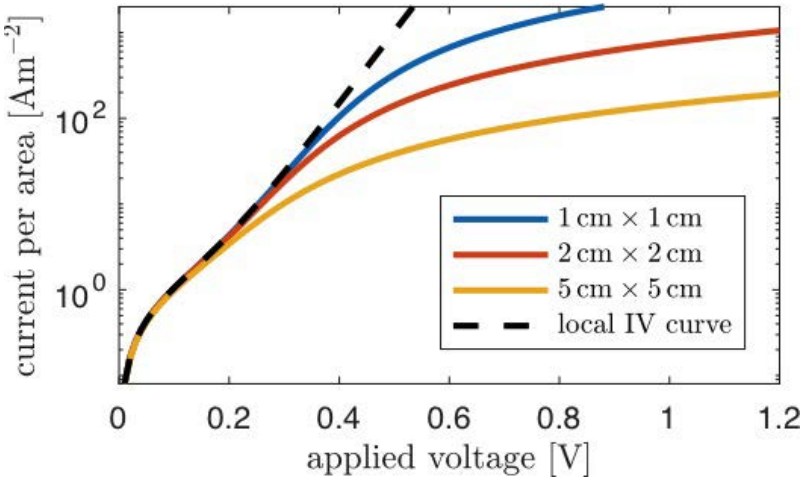
$$R^{\mathrm{th}}_{\square}(x,y) := (\lambda(x,y)d)^{-1}\,[\mathrm{KW}^{-1}/\square].$$

- Electrical→thermal:
  - Joule heating in the electrodes, $R^{\mathrm{el}}_{\square}{}^{-1}|\nabla\psi|^2$,
  - Joule heating in the semiconductor stack $\propto (1-\eta)|V j_s(V)|$, $V := \psi_t - \psi_b$.
- Thermal→electrical:

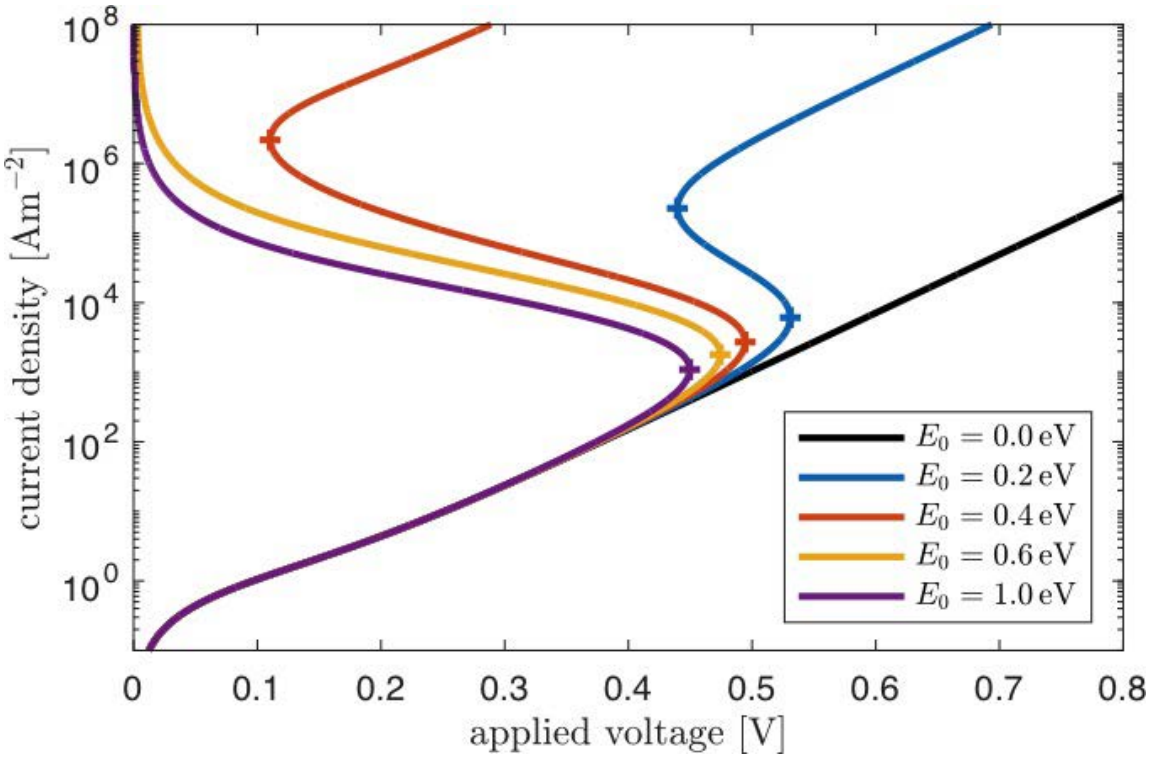


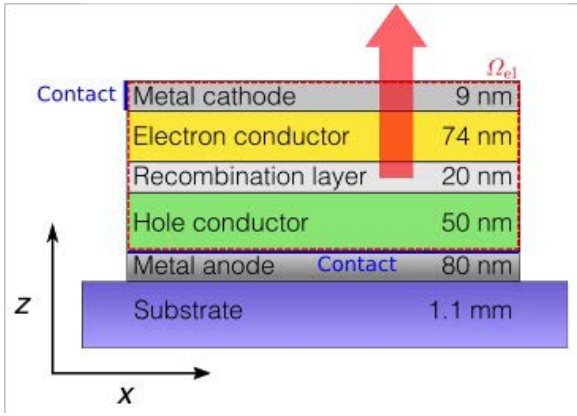
IV curves with negative differential resistance

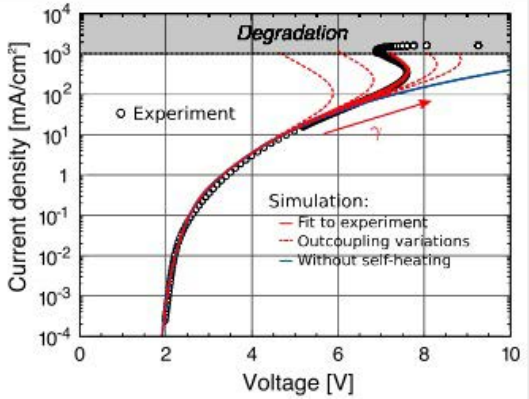
For a plain OLED device the electric current decreases with increasing device area (sheet resistance):



Together with thermal→electrical coupling we obtain S-shaped device-IV curves.







Liero et al., Opt Quant Electron, 2017

Conclusions and outlook

- We presented a coupled 0D-2D electrothermal model for the simulation of large-area semiconductor devices.
- Several experimental findings could be qualitatively reproduced.
- Simulation studies may help to explore new device-design ideas.

Some possible extensions:

- From steady-state model to transient and to AC models.
- More complex mathematical models for the semiconductor stack, p. ex. using a drift-diffusion model ($\rightsquigarrow$ coupled 1D-2D model).

Possible mathematical topic:

- Analytical/numerical investigation of the model-reduction error (3D $\rightarrow$ 0D-2D), depending on electrode thickness.