Zurich University of Applied Sciences
School of Engineering
InES Institute of Embedded Systems

Datasheet Radium Development Board

FPGA (with Hard Processor System)

Altera Cyclone V SoC	5CSXFC6D6F31C8NES
Logic Elements	110'000
LABs	41509
Memory	6191 kbit
I/Os	288
Transceivers (3.125 Gbps)	9
Variable Precision DSP Blocks	112
PCIe Hard IP	2
Hard Processor System	Dual ARM Cortex-A9
	10/100/1000 Ethernet MAC
	SDRAM Controller
	I2C, UART, CAN, SPI
	181 HPS IO
	UART on USB mini Connector
	MicroSD-Card Holder

SDRAM

Density	1Gbit (up to 4Gbit)
Data Rate	DDR3-1333

Flash Memory (1 x FPGA and 1 x HPS)

Density	256 Mbit
Interface	QSPI 108 MHz

Ethernet

Ethernet Ports	4 x 10/100/1000 RJ45
Chipset	Marvell 88E1543
Features	PTPv2, Auto-Media Detect
Internal Interface	SGMII to FPGA Transceivers

Extensions FPGA

Connector	HSMC 172 Pins (Class III reduced)
Transceivers (3.125 Gbps)	5 (PCIe support)
GPIO	Up to 20 LVDS channels or 80 CMOS
Additional Signals	I2C, JTAG, Differential Clocks

Extensions HPS

Connector	0.1” Reverse Polarity Protection
GPIO	20 Pins (SPI, UART, TRACE, GPIO)

Various

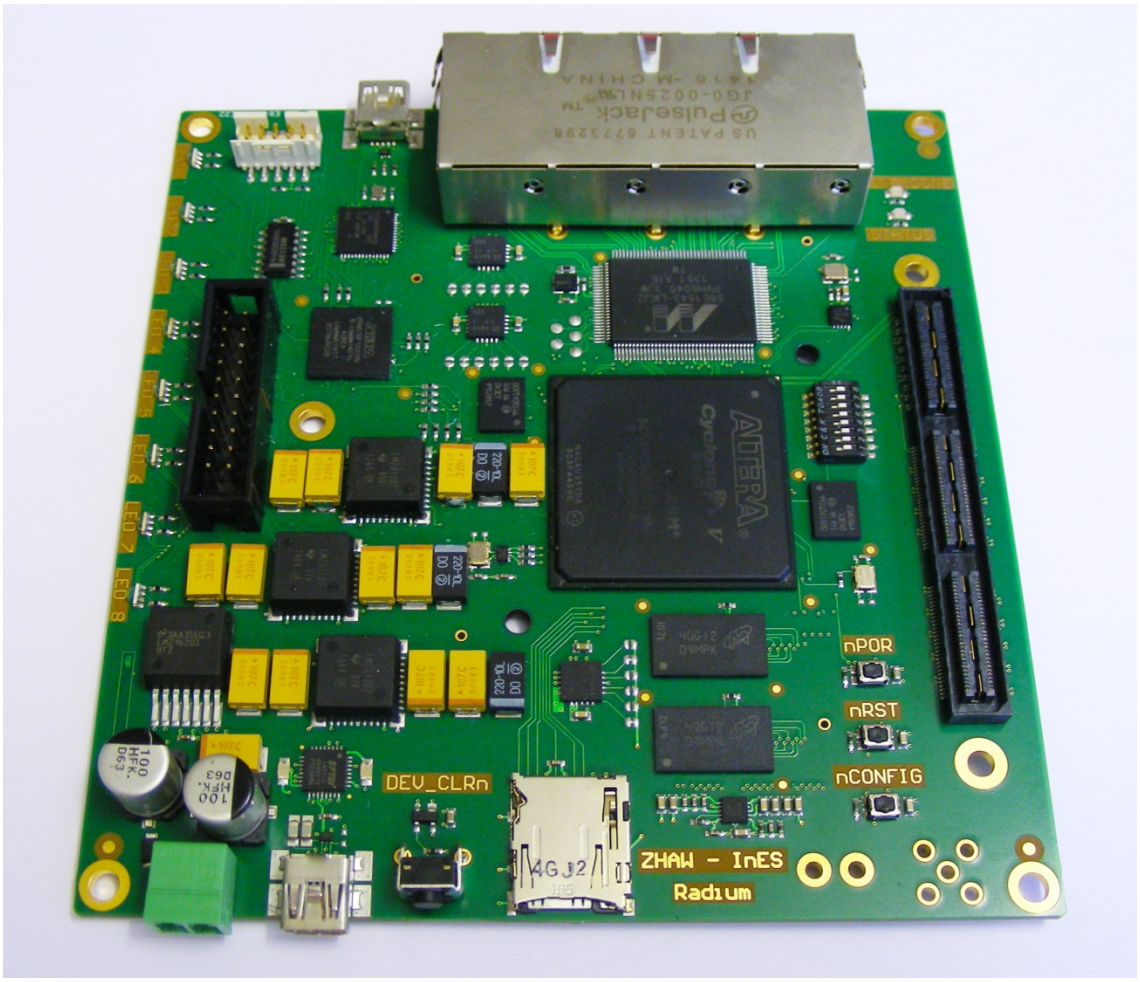
User-Definable	8 Bi-Color LED
Clock	Internal or External via SMA
Configuration	Built-In USB-Blaster II via USB mini or JTAG

Power Supply

Necessary Supply Voltage	12 – 24V
Power Dissipation	ca. 6 W (max. 28W)

Mechanical

Dimensions	120x115x16 mm


nPOR
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ZHAW - InES
Radium